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WDM Fiber Delay Lines and AWG Based Optical Packet Switch Architecture

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Abstract :In this paper authors discuss an optical packet switch (OPS) architecture which utilizes the components like optical reflectors, tunable wavelength converters (TWCs), arrayed waveguide grating (AWG) and pieces of fiber to realize the switching action. In this architecture AWG is used for routing purpose and symmetric nature of AWG simplify the switch operation effectively. It is also shown that using multi-wavelengths optical reflector, length of delay lines can be reduced to half of its original value. This diminution in length is useful for large size packets as for them length can grew up to more than few kilometers.

Keywords*:* AWG, TWC, optical reflectors, fiber delay lines.

I.INTRODUCTION

In the present days growing environment the internet plays a major role, and its significance grows rapidly. However as we know that the technological expansion of internet is very much difficult , that's why the one question arise that whether it will play a major role in solving diverse social problems or not , or whether it will become an transportation for generating a new approach for increasing the quality of life. As the time changes the new generation networks (NWGN) came in to existence as the replacement of internet to solve the above questions, and many of the research and development agencies worked to realize NWGN or more generally future networks. In the future networking technologies optical network is a very promising technology in the future networks.

Due to the massive bandwidth of optics, optical networking has been generally used to carry high volume of data in the core networks. In the present days optical communication system we generally uses the optical circuit switching (OCS) and due to the low recourse utilization OCS is not fit for bursty traffic of internet application. To resolve this problem in the past few years many of the researcher focused on this and we have seen many of the developments in the optical burst switching (OBS) and optical packet switching (OPS) networks, which provides more flexible options. The optical packet switching is a packet by packet switching with the help of OPS systems much broader bandwidth like 1 THZ or more can be easily and effectively managed.

In past, various optical packet switch architectures have been proposed. The architecture considered in [2] have simple routing algorithm, but structure of the switch is very complex and suffers from severe circulation limits. The architecture in [3] has simple buffering structure and routing algorithm but still control is required at the input, output as well as in the buffer. The architecture considered in [4] uses very large number of components, thus structure is very complex, but routing algorithm is very simple. The major disadvantage of the architecture is the large physical loss. In recent past architectures presented in [5] which have feed-forward and feed-backward type structures are extensively investigated as they provide low packet loss probability. The architecture presented here, will provide same packet loss performance as in [5] with much simpler buffering structure, and switch functionality can be achieved with very few components.

II. ARCHITECTURES DESCRIPTION

The architecture presented in [5] which has feedback architecture (A1) shown in Fig. 1(a) requires only one $2N\times2N$ AWG. It uses shared feedback delay lines to buffer the contended packets. First, input packets are converted to the appropriate wavelengths and the contended packets are routed to the re-circulating loops for buffering while the straight-through packets are routed to switch outputs. In the buffer only one packet may exit from each multiplexer in the loop at a time. No more than one packet may exit from each combination of fiber delay lines, a de multiplexer and a multiplexer; otherwise it will be routed to other alternative AWG outputs so it can be placed in other module or, if necessary to longer delay lines. Similarly in a single time slot only one packet can be inserted in each module.

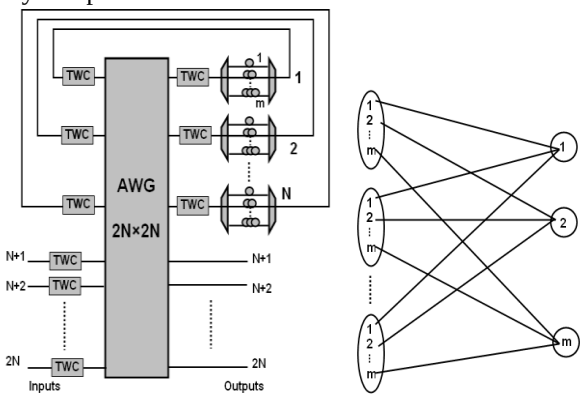

Fig. 1(a) Schematic of the architecture (A1) presented in [2]
(b) Schematic of the mapping structure

The switch consist of *N* modules one for each output port and for a tagged output at maximum *m* packets can be stored. Hence, in all the modules at maximum *N* packets can have same delay varying from 1 to *m* slots and in all the modules *mN* number of packets can be stored. The architecture can be simplified by doing proper mapping of

the packets and mapping structure is shown in Fig. 1(b), here, packets which require same delay (say q slots) will be stored in a common module (q) in shared manner. This will allow to eradicate the use of mux, demux and TWCs inside the buffer. In the proposed architecture A2 (Fig. 1(c)) the upper N ports of the AWG router ranging from 1 to N connect to N buffer modules. The lower ports (N+1 to 2N) of the AWG acts as actual inputs/outputs port of the switch which is equipped with TWCs and tune the wavelengths of the incoming packets as per the desired output ports. Suppose a packet arrives at the input i and destined for output j, and requires a delay of K slots. Then packet has to be pushed towards module K connected to the K^{th} port of the AWG. AWG is a cyclic wavelength router. The packet entering at the input port i can be routed to the output port K of the AWG by following the routing pattern of AWG,

$$\lambda(i,k) = \lambda_l$$
$$l = \left[1 + (i + k - 2) \bmod N\right] \quad (1)$$

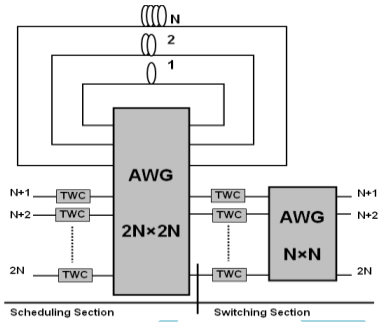

Fig 1(c) Schematic of the proposed architecture

A3after the delay of K slots packet will again appear at input of the scheduling AWG and get routed to output i of the AWG due to its symmetric nature and packet can be directed to the appropriate output (j) by tuning the wavelength through TWC in the switching section, by following routing nature of switching section AWG [6]. In the buffer, module 1 provides a delay of one slot, module 2 provide a delay of two slots and so on. Thus as per the required amount of delay packets can be placed in different modules. In each buffer module, only one packet per output port will be stored. Thus at most N packets can be stored for a particular output port in all the modules and in each module N wavelengths are used. This will allow storing/erasing of N packets in single time slot, one corresponds to each output. Referring 1 it can be calculated that, between consecutive modules, N-1 wavelengths are common. Therefore in N modules 2N-1 wavelengths will be required. Here, two types of buffer modules are considered. In the first type only pieces of fiber are used in the buffer, whose length varies from 1 to N slots.

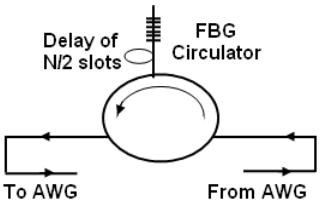

Fig. 2 Schematic of the buffer module

The second type of buffer module (Fig. 2) consists of one optical reflector, one circulator and pieces of fiber with length varies from 1/2 to N/2 slots. This reduction in length is useful for large size packets, where buffer delay line length can grow up to some kilometers. Optical reflector used in the different modules can be dielectric mirror, thin film based mirror and fiber Bragg grating (FBG) etc. The full description of the multi-wavelengths FBG is given in [7], where it is shown that, a large number of wavelengths can be reflected from a single grating. The reflectivity of the each wavelength in the entire reflection band is very high ~ 99.8%. The insertion loss of the device is negligible and also isolation is as high as ~ 50 dB. Further the grating is also helpful in dispersion reduction.

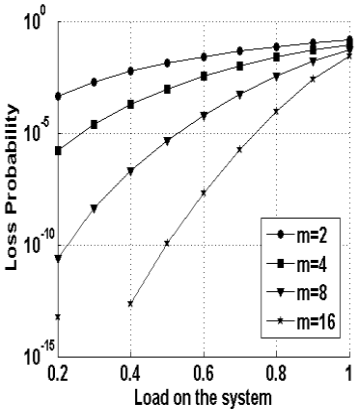

Fig. 3 Packet loss probability vs. load for different number of buffer module

In both the architectures, separate queue is formed for each output; therefore architecture can be modeled as output queued system. The length of the queue for the each output port will be decided by the number of modules (m) with maximum queue length of N packets. The performance evaluation of the output queued system is well described in [8], using the same model the results obtained for packet loss probability is shown in Fig. 3 for a switch of size N=16 and m varying from 2 to 16. It can be visualized from the figure even at higher load very low packet loss probability is attainable.

III. COMPARATIVE STUDY

In architecture A1 packets are buffered in optical time slot interchanger (OTSI), hence the architecture is bulky in nature and additionally no attention is paid for blocking OTSI. Along with this control algorithm for the switch is very complex. Controlling will required at three places i.e., input TWCs and two buffer TWCs. In the presented

architecture, structure and the routing algorithm is very simple, physical loss of the buffer is negligible and control will only be required only at the input and output of the

scheduling AWG. The unique feature of the architecture is that no controlling is required inside the buffer and using WDM a large number of packets can be stored in a single strand of fiber. Consider switch of size 16×16 with buffering capacity for each output of 16 packets. The typical loss of TWC and TF is 2 dB and for 16×16 mux and demux it is 5 dB. Hence, loss of each OTSI is 14 dB (neglecting fiber loss) which can be reduced to 7 dB (loss of TWC and AWG in switching section) in proposed architecture. In the proposed architecture buffer can be easily scaled by adding fiber delay lines this is contrast to architecture A1 where size of each OTSI has to be increased. The only advantage of the architecture A1 is that it is re-circulating in nature, but with the restriction that no incoming packet will contend with buffered packet for the same TWC placed before OTSI in single time slot. This re-circulating nature of the switch adds some flexibility in architecture.

A)Cost Analysis

The optical cost measure is considered as parametric estimate of cost, scalability and hardware requirements. The methodology and optical cost of various components follows form [9], where optical cost of the different components is obtained by counting fiber to chip coupling (FCC). But the cost of TWCs is considered to be 4 as FCC does not include the wavelength conversion range. To incorporate the effect of wavelength conversion a generalized cost model is proposed in [10], where the cost of the TWCs is given by the expression

$$C_{TWC} = ad^b \quad (2)$$

Here a is a normalization constant and d is the conversion range and the values of b lies between 0.5 to 5.

The optical cost of the architecture A1 can be given as

$$C_{A1} = NC_{TWC}^{in} + C_{AWG} + N\left[C_{TWC1}^{b} + C_{Demux} + C_{Mux} + C_{TWC2}^{b}\right] \quad (3)$$

Substituting the cost values of different components, we get

$$C_{A1} = N(2N-1)^b + 4N + N\left[(m-1)^b + m + 1 + m + 1 + (N-1)^b\right]$$

$$C_{A1} = N\left[(2N-1)^b + (N-1)^b + (m-1)^b + 2m + 6\right] \quad (4)$$

Similarly the cost of architecture A2 will be given by

$$C_{A2} = NC_{TWC}^{Sc} + C_{AWG}^{Sc} + NC_{TWC}^{sw} + C_{AWG}^{Sw} \quad (5)$$

After inserting cost values we get,

$$C_{A2} = N\left[(2N-1)^b + (N-1)^b + 6\right] \quad (6)$$

here the cost of the optical fiber is neglected in both the architectures, considering N=16 and m=16 and b=1 the cost values of architecture A1 and A2 will be 1584 and 832 FCC units. Hence, in the proposed architecture cost of the architecture is reduced by 48% still performance in terms of packet loss probability remains same. Similarly for b=0.5 the cost of architecture A1 is 832 and that of architecture A2 is 256 and hence cost reduction is 69%. Therefore, overall the proposed architecture is comparatively much better than the architecture A1.

IV.CONCLUSIONS

In this paper optical packet switch architecture is proposed, which is realized using components like optical reflectors, tunable wavelength convertor (TWC), arrayed waveguide grating (AWG) and pieces of fiber. This architecture uses routing pattern of AWG, and its symmetric nature, to simplify switch operation significantly. In the presented architecture, large number of packets can be stored in a single fiber delay line and in the buffer, controlling of the packets is not required. In OPS architectures, the physical limitations would be the number of components (e.g. SOA, AWG, TWC, MUX etc.) required to build the switch. In the proposed architecture, these limitations are eased as buffer is created by using very few components only.

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