# Comparative Analysis of Fully Depleted DMG SOI-MOSFET and SMG SOI-MOSFET

**Shikhar Gupta[1], Prashant Kumar[2], Anjali Chawla[3]**

[1,3]M.TECH Scholar, Dept. of Electronics Engineering, YMCAUST, Faridabad
[2]Assistant Professor, Dept. of Electronics Engineering, YMCAUST, Faridabad

***Abstract*-As the technology is improving there is a need of reducing the short channel effects and body effect. To reduce the body effect, the SOI-MOSFET is used instead of conventional MOSFET. A dual material MOSFET further improve critical parameters to the extent that these devices can be incorporated in integrated circuits at present. In this paper a dual material SOI-MOSFET is analyzed and its performance is compared with single material SOI-MOSFET. The threshold voltage and the sub-threshold swing were found to be reduced in the case of DMG SOI-MOSFET. The device is virtually fabricated and analyzed on ATLAS simulator of SILVACO TCAD Tools.**

***Keywords*: Silicon-on-insulator (SOI), single material gate (SMG), dual material gate (DMG), TCAD, MOSFET.**

## I. INTRODUCTION:

During the past few years, CMOS technology is improving its design and high speed performance with the use of high quality material and processing technology. In 1965, Gordon Moore proposed a law which described the evolution of the transistor density in integrated circuits. According to this law, the number of transistors per chip would become four times in every three years. So there is need of shrinking of the size of the transistor. The MOSFET dimensions have to shrink according to scaling law. However, with the reduction of the channel length, undesirable short channel effect arises which causes the dependence of device characteristics, such as threshold voltage on channel length. In contrast to the conventional bulk MOSFET devices, the SOI device has better control on its active silicon layer [1]; hence charge sharing effect is substantially reduced. The thin film SOI-MOSFETs offer good electrical characteristics over conventional bulk MOS devices.

In fully depleted SOI, the thickness of active silicon layer $t_{si}$ must be smaller than source/drain junction depth. In SOI devices, the distribution of non-uniform electric field occurred in the channel with the peak near the drain side. Thus, the charge carriers moving with a low velocity near the source [2], gradually accelerate towards the drain which results in the lower mean carriers transport velocity. When the channel length is small, than there is a probability of hot carrier effect due to high electric field peak near the drain [3]. There are many methods to reduce the SCE, such as use of tantalum gate, which adjust the threshold voltage without changing the doping densities. Double gate structure is also used to improve the SCE and the trans-conductance of the SOI devices [4].

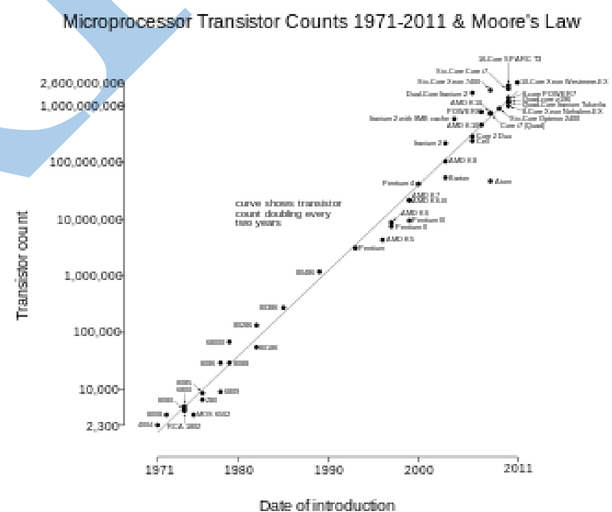


Figure1: Moore's Law

In a Dual Material Gate (DMG) SOI-MOSFET, two different materials with different workfunction are merged together. The workfunction of gate1 (M1) should be greater than the workfunction of gate2 (M2), i.e, $\phi_{M1} > \phi_{M2}$ [5] for n-channel SOI-MOSFET; and $\phi_{M2} > \phi_{M1}$ for p-channel SOI-MOSFET. This result in the formation of potential drop inside the channel, which cause in reduction of the SCEs and uniform electric field distribution along the channel[6].

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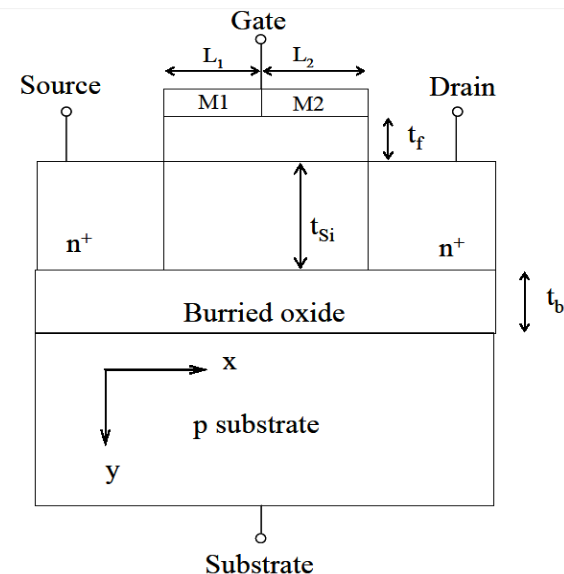


Figure 2: Cross sectional view of fully depleted DMG SOI-MOSFET

In this paper, a DMG SOI-MOSFET is designed using Silvaco TCAD Tools. The electrical characteristics of the device; such as threshold voltage, sub-threshold swing is compared with the SMG SOI-MOSFET

## II. DEVICE SPECIFICATIONS

The single material gate SOI MOSFET structure is shown in Fig 3(a) and dual material gate FD SOI MOSFET structure is as shown in Fig. 3(b). The channel length is 60nm; the lengths of source and drain are 60nm. The thickness of oxide layer is 2nm. The thickness of Silicon layer is 5nm. The thickness of buried oxide layer is 50nm. Half of the gate is made up of Aluminium and half of the gate is made up of n-type polysilicon layer. One half of the gate near the source side is made up of Aluminum and the other half of the gate is made up of n-type polysilicon.

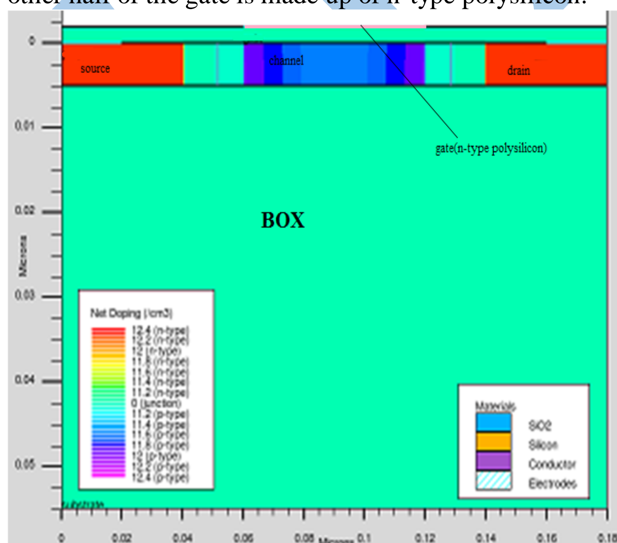


Figure 3(a): A 60nm FD SMG SOI-MOSFET

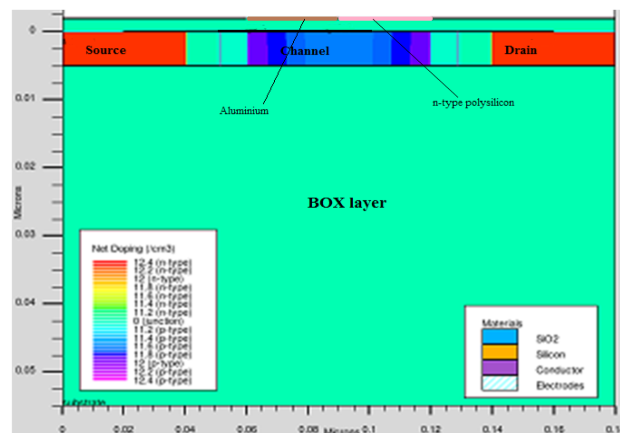


Figure 3(b): A 60nm FD DMG SOI-MOSFET

## III. DEVICE SIMULATION

On applying the gate voltage of about 0.4 V and a drain voltage of about 0.1V, the drain current varies almost linearly along the gate voltage. The substrate is kept at zero voltage. The graph shown below shows the variation of drain voltage with respect to the gate voltage. Here, the gate voltage is initialized with a voltage of 0.1V and there is an increment of 0.1V upto 1.5V. The figure 4 shows the threshold voltages curve. The maximum slope of this curve shows the threshold voltage. The figure 5 shows the subthreshold characteristics of the device.

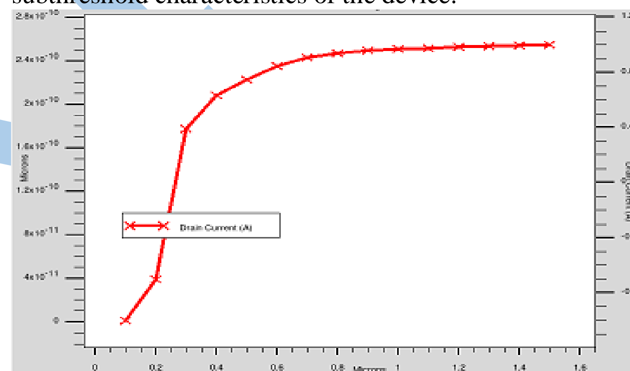


Figure 4(a): Threshold Slope of 60nm FD SMG

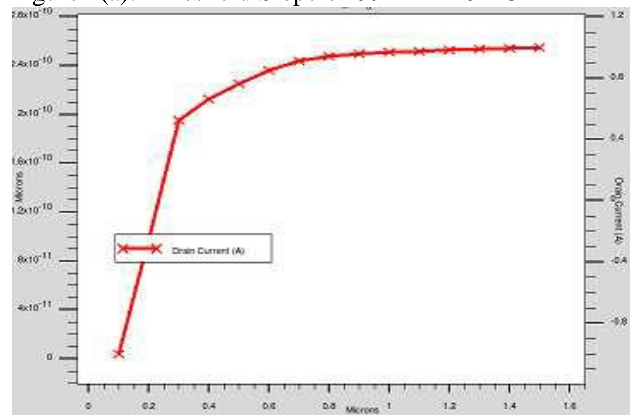


Figure 4(b): Threshold Slope of 60nm FD DMG SOI-MOSFET

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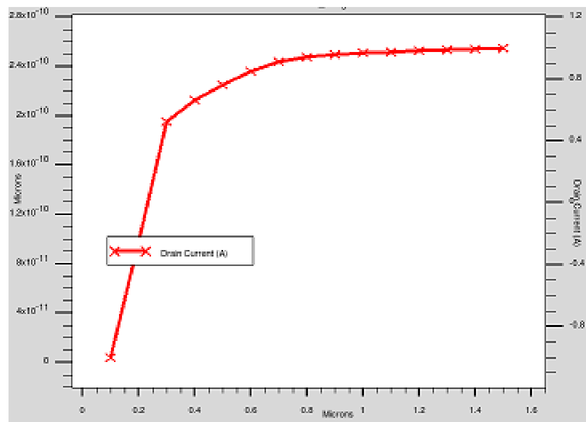


Figure 5(a): Subthreshold slope of 60nm FD SMG-SOI MOSFET

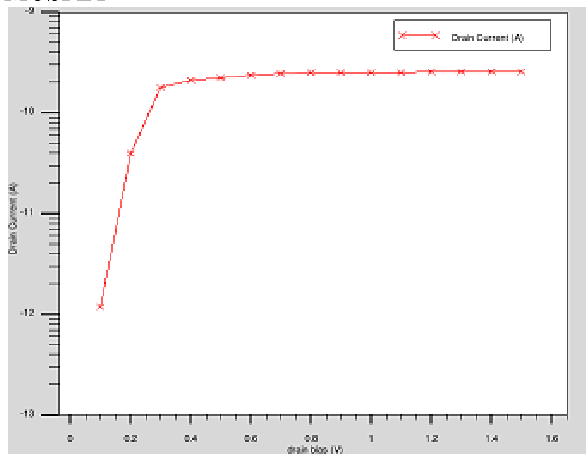


Figure 5(b): Subthreshold Slope of 60nm DMG SOI-MOSFET.

## IV. RESULT

| Parameter | SMG | DMG |
|---|---|---|
| Threshold Voltage | 0.122008 V | 0.0494949 V |
| Sub-threshold Swing | 0.0660585 V/decade | 0.0710692 V/decade |
| Drain current | 1.24579e-13 A | 1.60322e-09 A |
| DIBL | 0.004416 V/V | 0.00126166 V/V |
| $I_{ON}/I_{OFF}$ | 2045.58 A/A | 785.57 A/A |

The above table shows the comparisons of the various parameters for fully depleted SMG and DMG SOI-MOSFET. It is clear that the parameters are improving by using the dual material gate instead of using single material gate.

## V. CONCLUSIONS

An dual material and single material SOI device on 60nm is designed and simulated on Silvaco TCAD, critical parameters were extracted for analysis. The threshold voltage improvement was observed in the dual materials SOI device, other than this DIBL, Drain current and $I_{ON}/I_{OFF}$ was also found in DM-SOI devices. The subthreshold swing was observed to be increased with DMG-SOI devices, all these improvements in these critical parameters can be attributed to dual material which is applied in the gate while fabrication. Hence using a DMG-SOI will result in the improvement in the parameters with a bit of design complexity for the integrated circuits of the future. The type of poly-silicon material also affects the performance of the device.

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