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Design and Implementation of High Speed Carry Select Adder

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Abstract—Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. From the structure of the CSLA, it is clear that there is scope for reducing the delay and increase the speed in the CSLA. This work uses a simple and efficient gate-level modification to significantly reduce the delay and increase the speed of the CSLA. Based on this modification16-b square-root CSLA (SQRT CSLA) architecture have been developed and compared with the regular SQRT CSLA architecture. The proposed design has reduced delay as compared with the regular SQRT CSLA with only a slight increase in the area and power.This paper proposes an efficient method which replaces the BEC using D latch. Experimental analysis shows that the proposed architecture achieves the one advantage in terms of delay.

***Index Terms*— CSLA, speed, delay,BEC.**

I. INTRODUCTION

A carry-select adder is divided into sectors, each of which – except for the least-significant –performs two additions in parallel, one assuming a carry-in of zero, the other a carry-in of one. A four bit carry select adder generally consists of two ripple carry adders and a multiplexer. The carry-select adder is simple but rather fast, having a gate level depth of Adding two n-bit numbers with a carry select adder is done with two adders (two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known [4].

Low-power, area-efficient, and high performance VLSI systems are increasingly used in portable and mobile devices, multi standard wireless receivers, and biomedical instrumentation [2]. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position [1].

The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum .However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input cin = 0 and cin = 1, then the final sum and carry are selected by the multiplexers (mux).The power and Area of the Carry select Adder can be reduced by using BEC-1 converter instead of Ripple Carry Adder(RCA). [1], [3].

The basic idea of this work is to use Binary to Excess-1 Converter (BEC) instead of RCA with cin = 1 in the regular CSLA to achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure [1], [3].

II. RIPPLE CARRY ADDER (RCA)

The ripple carry adder is constructed by cascading full adders (FA) blocks in series. One full adder is responsible for the addition of two binary digits at any stage of the ripple carry. The carryout of one stage is fed directly to the carry-in of the next stage. Even though this is a simple adder and can be used to add unrestricted bit length numbers, it is however not very efficient when large bit numbers are used. One of the most serious drawbacks of this adder is that the delay increases linearly with the bit length. The worst-case delay of the RCA is when a carry signal transition ripples through all stages of adder chain from the least significant bit to the most significant bit, which is approximated by: $t = (n -1)tc + ts$.. Eq (1) where tc is the delay through the carry stage of a full adder, and ts is the delay to compute the sum of the last stage. The delay of ripple carry adder is linearly proportional to n, the number of bits, therefore the performance of the RCA is limited when n grows bigger. The advantages of the RCA are lower power consumption as well as compact layout giving smaller chip area. The design schematic of RCA is shown in Figure (1).

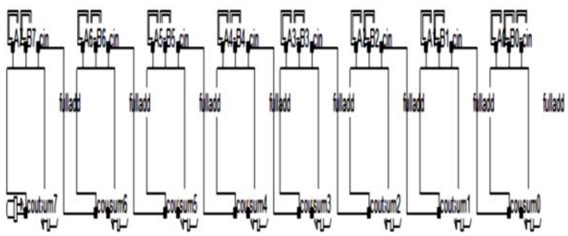

Figure 1 Schematic of RCA

III. BEC

As stated above the main idea of this work is to use BEC instead of the RCA with cin = 1in order to reduce the area and power consumption of the regular CSLA. To replace the n-bit RCA, an n+1-bit BEC is required. A structure and the function table of a 4-b BEC are shown in Fig. 2 and Table I, respectively. Fig. 3 illustrates how the basic function of the CSLA is obtained by using the 4-bit BEC together with the mux. One input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two possible partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal Cin. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed. The Boolean expressions of the 4-bit BEC is listed as (note the functional symbols ~NOT, & AND,’ XOR).

X0=~B0
X1=B0’B1
X2=B2’ (B0 & B1)
X3=B3’ (B0 & B1 & B2)

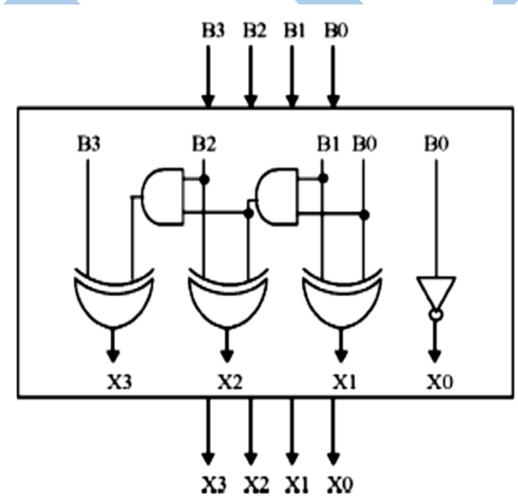

Figure 2 4-b BEC.

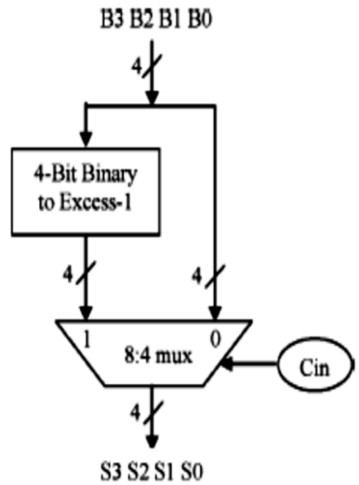

Figure 3 4-b BEC with 8:4 Mux.

TABLE-I FUNCTION TABLE OF THE 4-B BEC

B [3;0]	X[3:0]
0000	0001
0001	0010
-	-
-	-
-	-
1110	1111
1111	0000

IV. REGULAR 16-BIT SQRT CSLA

Design of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of res earch in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after t he previous bit position has been summed and a carry pro pagated into the next position .The CSLA is used in man y computational systems to alleviate the problem of carry propagation delay by independently generating multiple c arries and then select a carry to generate the sum. The car ry-select adder (CSLA) provides a compromise between small area but longer delay ripple carry adder (RCA) and larger area with shorter delay carry look-ahead adder. CS LA uses multiple pairs of ripple carry adder (RCA) to ge nerate partial sum and carry by considering carry input C in=0 and Cin=1, then the final sum and carry are selected by multiplexers.

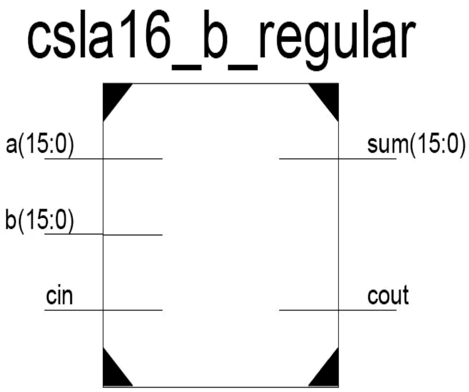

Figure 4. Block Diagram of Regular CSLA

Above fig. is the Block Diagram of REGULAR CSLA where a (15:0), b (15:0) and cin are the Inputs a, b are 16-bit inputs and cin are 1-bit inputs. Same as sum (15:0) and cout are Outputs [1].

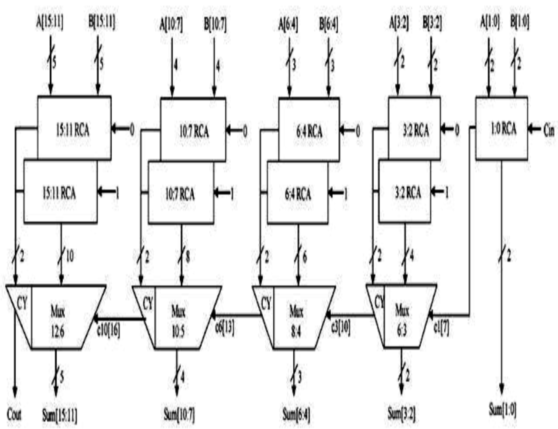

Figure 5. 16-bit SQRT Regular Carry Select Adder

V. MODIFIED CSLA USING BEC

The structure of the modified 16-b SQRT CSLA using BEC for RCA with Cin=1 to optimize the area and power is shown in Figure 6. We again split the structure into five groups. One input to the mux goes from the RCA with Cin=0 and other input from the BEC. Comparing the both regular and modified CSLA, it is clear that BEC structure reduces the area and power. The Parallel RCA with Cin=1 is Replaced with BEC. [1][7]

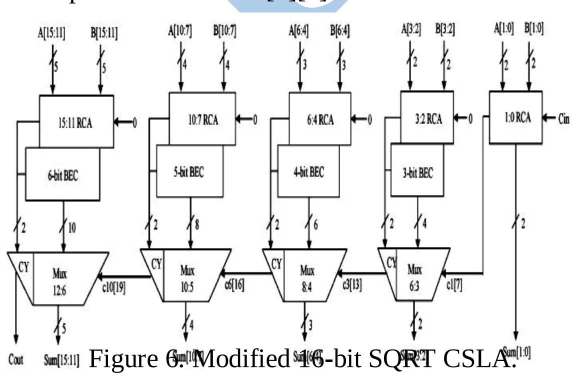

Figure 6. Modified 16-bit SQRT CSLA.

VI. D-LATCH

This latch exploits the fact that, in the two active input combinations (01 and 10) of a gated SR latch, R is the complement of S. The input NAND stage converts the two D input states (0 and 1) to these two input combinations for the next SR latch by inverting the data input signal. The low state of the enable signal produces the inactive "11" combination. Thus a gated D-latch may be considered as a one-input synchronous SR latch. This configuration prevents application of the restricted input combination. It is also known as transparent latch, data latch, or simply gate d-latch. It has a data input and an enable signal (sometimes named clock, or control). The word transparent comes from the fact that, when the enable input is on, the signal propagates directly through the circuit, from the input D to the output Q. [7]

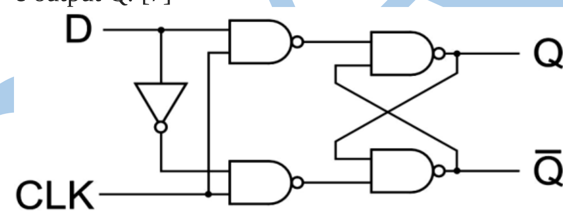

Figure 7. D-latch

Truth Table shown below explains the operation of D-latch according to applied Input. SET and RESET condition are defining the working. According to clock signal value the Input pass to the Output

TABLE 2. Truth Table of D-latch

$\overline{SET}$	$\overline{RESET}$	D	CK	Q	$\overline{Q}$
0	1	-	-	1	0
1	0	-	-	0	1
0	0	-	-	1	1
1	1	1	↑	1	0
1	1	0	↑	0	1

The Waveform of D-latch is shown below in fig. Here E is enable signal work as clock signal on which Output value are depends

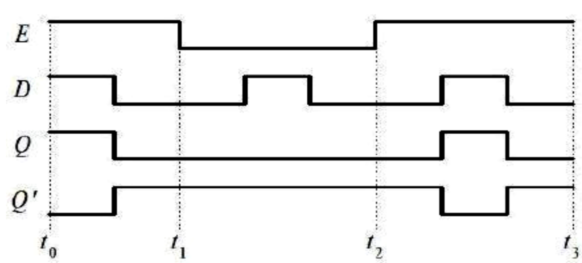

Figure 8. Input and Output Waveforms

VII. PROPOSED 16-BIT CSLA USING D-LATCH

This method replaces the BEC add one circuit by D-latch with enable signal. Latches are used to store one bit infor mation. Their outputs are constantly affected by their inp uts as long as the enable signal is asserted. In other words , when they are enabled, their content changes immediate ly according to their inputs. [7] The architecture of propo sed 16-b CSLA is shown in Figure 9. It has different five groups of different bit size RCA and D-Latch. Instead of using two separate adders in the regular CSLA, in this me thod only one adder is used to calculate the area, power c onsumption and delay. Each of the two additions is perfo rmed in one clock cycle. This is 16-bit adder in which lea st significant bit (LSB) adder is ripple carry adder, which is 2 bit wide. The upper half of the adder i.e. most signifi cant part is 14-bit wide which works according to the ``cl ock. Whenever clock goes high addition for carry input o ne is performed. When clock goes low then carry input is assumed as zero and sum is stored in adder itself. From th e Figure 9. it can understand that latch is used to store the sum and carry for Cin=1 and Cin=0.Carry out from the pr evious stage i.e, least significant bit adder is used as contr ol signal for multiplexer to select final output carry and s um of the 16-bit adder. If the actual carry input is one, the n computed sum and carry latch is accessed and for carry input zero MSB adder is accessed. Cout is the output carr y.

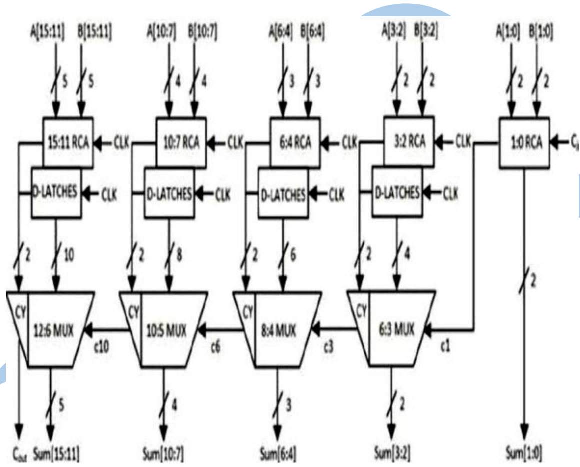

Figure 9. Modified CSLA using D-latch

VIII. SIMULATION RESULTS OF ADDERS

With the help of test bench, one can see the waveform of a design by giving different input combination. Test benc h is provided to see the output values by giving input valu es and it is simulated on a simulation tool. We are simula ting test benches on Xilinx ISE.

The output gives values at every positive edge of clock si gnal. If input is changing in mid of clock signal then outp ut is modified only at positive edge of clock signal. Simu lation results for all adders are given below

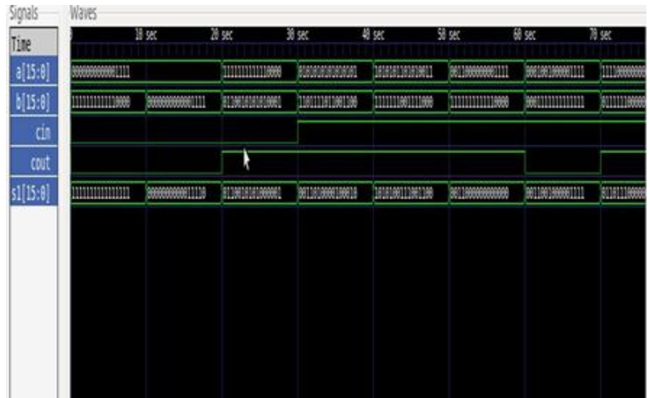

Figure 10.Waveform of Regular CSLA

Figure 11. Waveform of CSLA using BEC

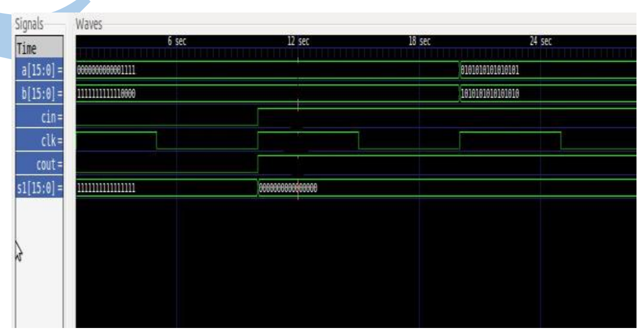

Figure 12. Waveform of CSLA with D-latch

IX. CONCLUSION

Power, delay and area are the most prominent factors i n VLSI design that limits the performance of any circui t. This work presents a simple approach to reduce the d elay and increase the speed of CSLA architecture. The conventional carry select adder has the disadvantage of more power consumption and occupying more chip are a. The modified CSLA reduces the area, delay and pow er when compared to regular CSLA by the use of Binar y to Excess-1 converter. This paper proposes a scheme which reduces the delay, but increase the area and pow er than regular and modified CSLA by the use of D-lat ches.so if anyone want to use the high speed carry sele ct adder then they have option to use CSLA with BEC, and also use CSLA with D-latch for the fast calculation on the price of area and delay. The comparative analysi s for all adders is shown in table which is given below:

TABLE 3. Comparison of Various Parameters

Adder	Regular C SLA	CSLA wi th BEC	CSLA with D Latch
Power Dissipation (n w)	10748.698	10253.90 6	12786.4 58
Dealy(ns)	10.073	9.794	8.254
No.of Luts	43/12288	43/12288	50/1228 8
Lut utilization	0.35%	0.35%	0.4%
No.of occupie d slice	25/6144	24/6144	36/6144
Slice Utilizati on	0.4%	0.39%	0.58%

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