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Impact of Potential Induced Degradation on Solar PV Module

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Abstract: **Since solar energy generation is getting more and more important worldwide PV systems and solar parks are becoming larger consisting of an increasing number of solar panels being serially interconnected. As a consequence panels are frequently exposed to high relative potentials towards ground causing High Voltage Stress (HVS). Depending on the technology different types of Potential Induced Degradation (PID) occur. This paper is focusing on PID of wafer based standard p-type silicon technology aiming on increasing life times for solar panels once exposed to external potentials in the field. A test setup is presented for simulation of the PID in the lab and the influence of cell properties on PID is demonstrated in order to reveal the cell being the precondition for the PID. However, PID can also be stopped or minimized on panel and system level as shown in the paper.**

Keywords: Solar PV Module, HVS, PID

I. INTRODUCTION

Differences of up to one thousand volts occur between the ends of a string. For safety reasons, all metallic frames of the modules have to be grounded at a fixed potential. This leads to a voltage bias of the individual string units with respect to their frames. This bias can cause a leakage current flow between the frame and the solar cells and can have negative impact on the long time performance of PV panels and systems. This degradation mechanism is called potential induced degradation (PID)[9]. Potential-induced degradation (PID) can be understood as a designation for aging effects which arise due to the potential difference between cells and earth. In the past, a form of PID which can lead to a decrease in power has been observed for crystalline PV modules, without the module having externally visible damage[14]. Due to the voltage between cells and earth (frame / front glass cover), positive ions can migrate into the solar cell, for example, reducing the output power. At present, we are investigating this effect on live solar panels in the field [13].

II. EXPERIMENTAL

Potential induced degradation (PID) of crystalline silicon modules, if the cells are on negative potential against ground [13]. Worst case would then be -1000V for grounding the positive pole of the inverter. High rates of PID were observed when the outer surface of the module became electrically conductive forming the ground electrode against negative cell bias. This effect is caused by surface humidity in real operation and can be simulated in climatic cabinets, by applying wet cloth, or highly conducting layers on the glass panes (aluminium foils). The high potential causes a leakage current that might be a measure for the degradation rate [9].

III. EXPERIMENTAL RESULTS

System level

The following example (fig.1) shows an EL image of a floating system that is affected by PID. The arrow indicates the rising system voltage. When going from negative potential (left) to positive potential (right) versus ground. Degradation stops when the potential turns from negative to positive

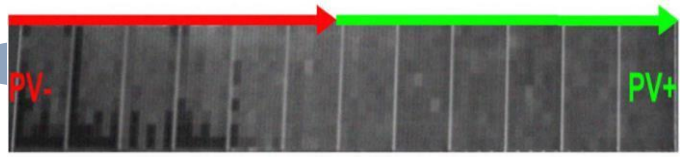

Figure 1: EL image of a floating PIO string with degraded panels on the side with negative potential.[13]

In case the potential is not floating but fixed in the way that the PV- pole of the string is grounded PIO can be effectively prevented. However, in the last years inverter development was resulting in higher efficient technologies partly due to the abandonment of transformers. As a consequence grounding is not possible and PID has to be prevented with another approach.

Panel level

Taking a closer look at the PID effect on the panel level as done in case of prone solar cells in a standard panel – see the following EL images before and after the PID test with 1000V for 100hr. First in general the brightness of the picture is decreasing (not visible here) and second single cells are not uniformly affected. Some cells degrade heavily and seem to be short circuited while others appear to be stable. The reasons for this variation must be investigated on cell level as will be done in the next chapter.

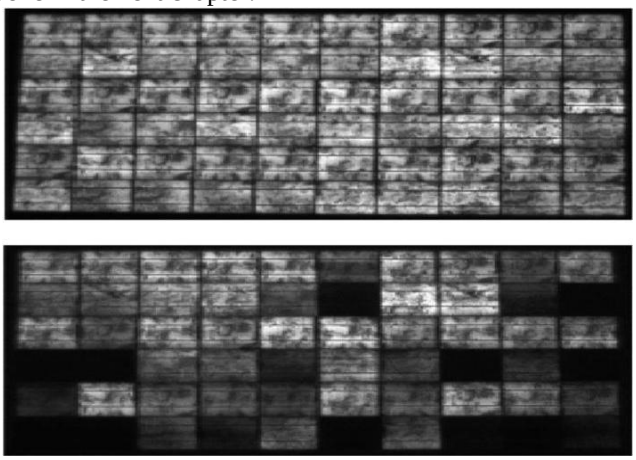

Figure 2: EL image of a panel before (upper) and after (lower)

100hr 1000V PIO test - power loss was 32% [9].
In order to minimize or avoid PID on panel level and therefore to increase life time and reliability the appropriate material combination have to be found making sure that solar cells prone to PID are combined with ENG materials resulting in low leakage currents on panel level. There are alternative materials to standard EVA better performing in respect to PID but other criteria like price, handling, long term stability issues and availability have to be taken into account. So although it was shown that it is possible to suppress PID in case of prone cells by switching the ENG material it seems to be even more favourable to minimize or avoid PID on cell level which is discussed in the following chapter.

Cell level

The following two graphs show the evolution of the IV curve with ongoing PID and the corresponding power degradation over time

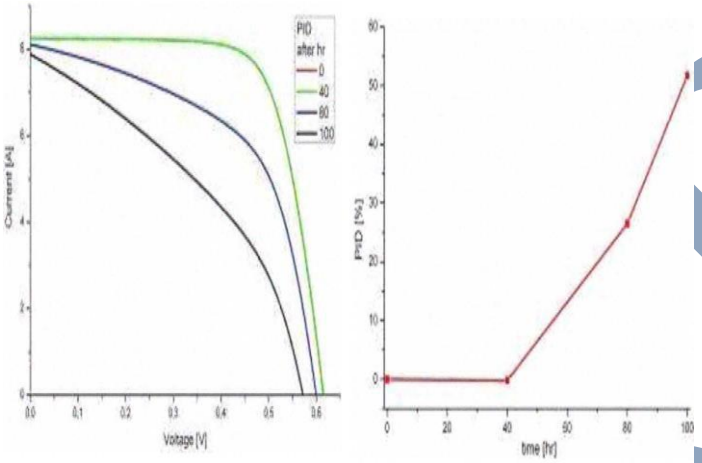

Figure 3: PID IV curve evolution (left) and corresponding power degradation (right). [14]
In case of PID shunt resistance as well as the reverse bias current is affected first followed by FF. Finally Voc decreases reflecting the junction to be less capable of separating holes and electrons.

Time	Uoc	Isc	P	FF	I(-12v)	Rsh
[hr]	[V]	[A]	[W]	%	[A]	[ohm]
0	0.615	8.240	3.616	71.4	0.21	80.4
40	0.615	8.258	3.622	71.3	0.30	51.1
80	0.600	8.109	2.658	54.6	>10	0.5
100	0.572	7.882	1.746	38.7	>10	0.2
Rel. PID	-7%	-4%	-52%	-46%	_	-100%

Table 1: Cell IV key parameter change during PID.

The Isc is the parameter that is least affected but with advancing PID Isc also degrades. Depending on the degree of PID the junction is loosing its blocking characteristic under reverse bias or totally breaks down (ohmic shunt). This phenomenon can be visualized by EL images taken during a PID test that are shown in the upper row. After 40hr local shunts appear along the edge of the cell that degrade further from diode to ohmic behaviour, as can be seen in the reverse bias image in the lower row. First shunted areas appear bright but after further PIO evolution these areas do not emit any more breakdown light [6]. Finally after 100hr both images are dark because of dominating ohmic shunts.

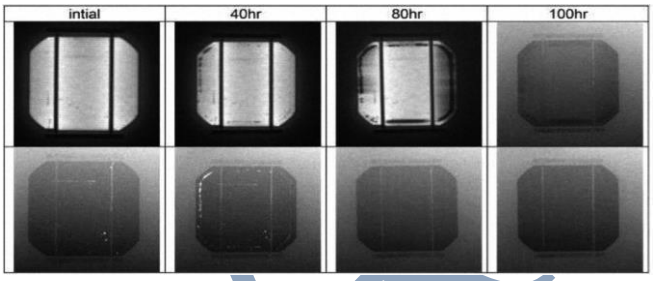

Figure 5: EL image of a cell during PIO test (upper row) and reverse bias (-12V) image (lower row).[12]

The leakage current in form of electrons or ions is resulting in an increased charge concentration above the solar cell in the ENG. These charges interact with the emitter and depletion layer and disrupt their function. From semiconductor industry similar effects are known as (time dependent) dielectric breakdown or surface inversion [5]. The electric field of these charge carriers is influencing the p-n junction in that way that junction gets more conductive and the local shunt resistance drops. Sunpower applied a transistor model to the polarization effect [4] on their ntype back contact cell. In the case of standard p-type cells this model also works but the configuration needs to be switched from npn- to pnp-transistor. There are numerous factors on cell level being important in respect to PID. In the following we present the parameters indentified to have a significant impact [13].

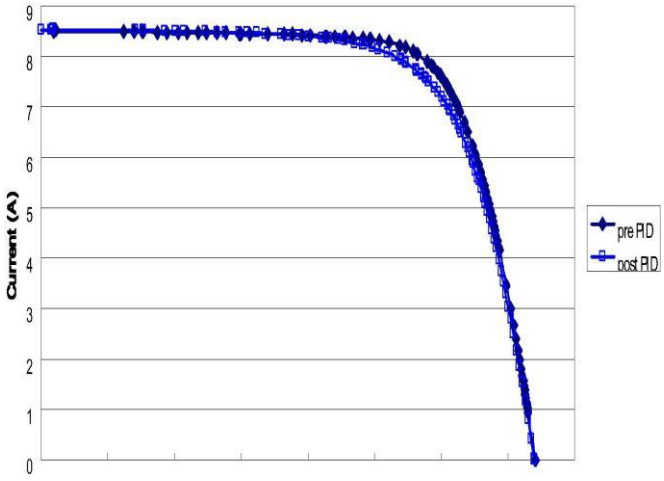

Figure 4: IV curve pre PID and post PID test.[14]

Further more, in order to identify the PID property we applied a 1000V reverse bias relative to PID test. We found the power recovery by reverse potential during 0.05hr continuous test as

showed in Table 2 and Figure 4 IV curves. It showed fill factor apparent to go back to 72.199% after 0.05hr reverse potential performance. In figure 5 also showed the recovery EL image which the dark areas almost disappeared after a reverse voltage compared with Figure 2 (right). It also revealed the polarization effect in our case and no corrosion effect.Figure 6:The recovery IV curve after applied 1000V reverses potential.[13]

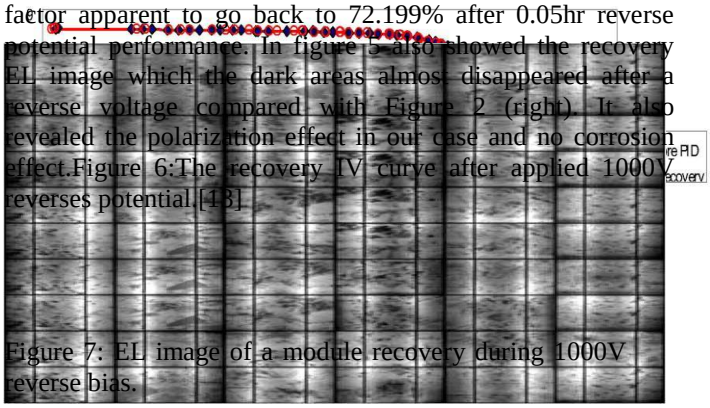

Figure 7: EL image of a module recovery during 1000V reverse bias.

CONCLUSION

This paper presented a degradation mechanism called Potential Induced Degradation (PID) that is getting more important with growing PV system sizes going along with higher system voltages. It was shown that - although the origin of PID is on cell level - it can be minimized or avoided on all levels - system, panel and cell. The solution on system level is choosing an appropriate grounding scheme of the string poles while on panel level

the properties of the encapsulation material determine the height of leakage currents that can in case of prone solar cells lead to PID. On cell level many parameters influence the PID stability of solar cells. Besides base material resistivity and emitter sheet resistance the most important parameter was found to be the anti-reflective coating since adaption of this layer can avoid the effect of PID. The PID effect can be reversed by switching the polarity and also high temperatures support regeneration. Also use of PV offset box or a galvanically isolating inverter and a negative earthing set is highly effective to overcome PID.

Taking these findings into account long term stability of solar panels can be significantly improved by adapting processes on all levels in order to minimize PID and therefore optimize the energy output of the PV system over a 25+ year life time.

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